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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,900	09/22/2003	Kazi Asaduzzaman	174/277	2500

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,900	ASADUZZAMAN ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-25* is/are allowed.

6)☒ Claim(s) *1-19 and 26-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 9, 12-19, 26-28, 32-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Groen et al U.S. Patent No 6,956,441 B2.

As per claims 1 and 26 Groen et al teaches an apparatus for receiving and processing a clock data recovery (CDR) signal comprising: reference clock signal processing circuitry (see fig.4a element 112) that receives as input a reference clock signal (see fig.4a element 86) and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal; data recovery circuitry (see fig.4a element 110) that receives as input the recovered clock signal (see fig.4a element 138) and the CDR signal and is operative to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover data information in the CDR signal (see col7, lines 1-50); and control circuitry (see fig.4a element 100) that receives as input a first signal and a second signal (see fig.4a elements 126-130) and is operative to

control the reference clock signal processing circuitry and the data recovery circuitry (see col.7, lines 3-50).

As per claim 2, Groen et al teaches wherein the reference clock signal processing circuitry comprises a divider circuit (see fig.4a element 120) that divides the recovered clock signal by a predetermined scale factor.

As per claim 3, Groen et al teaches wherein the reference clock signal processing circuitry further comprises: a phase frequency detector that compares (see fig.4a element 114) the phase and frequency of the reference clock signal and an output signal of the divider circuit, and outputs a signal indicative of whether the output signal of the divider circuit should be speeded up or slowed down to better match the phase and frequency of the reference clock signal.

As per claim 9, Groen et al teaches wherein the data recovery circuitry (see fig.4a element 102) further comprises a phase detector (see fig.4a element 114) that compares a phase of the recovered clock signal and the CDR signal and outputs a signal indicative of whether the recovered clock signal needs to be speeded up or slowed down to better match the phase of the CDR signal.

As per claim 12, Groen et al inherently teaches wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry: first, directs operation of the reference clock signal processing circuitry; and second, directs operation of the data recovery circuitry in response to receiving an output signal from the reference clock signal processing circuitry indicating that the

recovered clock signal has a phase and frequency similar to the phase and frequency of the reference clock signal.

As per claim 13, Groen et al inherently teaches wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry directs operation of the reference clock signal processing circuitry.

As per claim 14, Groen et al inherently teaches wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry directs operation of the data recovery circuitry.

As per claim 15, Groen et al inherently teaches wherein the first signal and the second signal are set by at least one of programmable logic resource core circuitry, circuitry external to programmable logic resource core circuitry, or user input.

As per claim 16, Groen et al teaches and A digital processing system comprising: processing circuitry; a memory (see fig.2 element 45) coupled to the processing apparatus as defined in claim 1 coupled to the processing circuitry and the memory.

As per claim 17, Groen et al inherently teaches printed circuit board on which is mounted the apparatus as defined in claim 1.

As per claim 18, Groen et al inherently teaches further comprising: a memory mounted on the printed circuit board and coupled to the apparatus.

As per claim 19, Groen et al inherently teaches further comprising: processing circuitry mounted on the printed circuit board and coupled to the apparatus.

As per claims 27 and 34, Groen et al teaches wherein processing the reference clock signal and the CDR signal comprises: processing in reference clock mode to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal (see fig.4a element 112); and processing in data mode to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover the data information in the CDR signal (see fig.4a element 110).

As per claim 28, Groen et al teaches wherein the processing in reference clock mode and the processing in data mode are controlled by a first signal and a second signal (see fig.4a elements 126-130).

As per claim 32, Groen et al inherently teaches further comprising processing in reference clock mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

As per claim 33, Groen et al inherently teaches further comprising processing in data mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

As per claim 19, Groen et al teaches wherein processing the different reference clock signal and the different CDR signal comprises: processing in reference clock mode to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal (see fig.4a element 112); and processing in data mode to phase align the recovered clock

signal to the different CDR signal, to use the recovered clock signal to recover clock information embedded in the different CDR signal, and to use the clock information to recover the data information in the different CDR signal (see fig.4a element 110).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-8, 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groen et al U.S. Patent No 6,956,441 B2 in view of Johansen U.S. Patent No 6,631,144.

As per claims 4 and 10, Groen et al teaches all the features of the claimed invention except for wherein the reference clock signal processing circuitry further comprises: a charge pump that receives as input the output signal of the phase frequency detector; and a loop filter that receives as input the output of the charge pump to produce a voltage controlled oscillator current control signal.

Johansen teaches reference clock signal processing circuitry further comprises: a charge pump that receives as input the output signal of the phase frequency detector; and a loop filter that receives as input the output of the charge pump to produce a voltage controlled oscillator current control signal (see figs.2-3 elements 440 and 430 and col.16, lines 45-67 and col.17, lines 50-67).

It would have been obvious tone of ordinary skill in the art to implement the teaching of Johansen into Groen as to assure that the DCR would always be kept within its lock-in range in relation to an expected bit rate of the incoming data stream as taught by Johansen (see col.18, lines 1-15).

As per claims 5 and 11, Groen and Johansen in combination would teach wherein the reference clock signal further comprises: a voltage controlled oscillator that receives as input the voltage controlled oscillator current control signal and outputs the recovered clock signal that better matches the phase and frequency of the reference clock signal as to assure that the DCR would always be kept within its lock-in range in relation to an expected bit rate of the incoming data stream as taught by Johansen (see col.18, lines 1-15).

As per claim 6, Johansen teaches wherein the reference clock signal processing circuitry further comprises: a lock detector that receives as input the output signal of the phase frequency detector and outputs a signal indicative of whether a phase of the output signal of the divider circuit is similar to the phase of the reference clock signal (see figs.2-3 element 425 and col.17, lines 23-26, 63-67).

It would have been obvious tone of ordinary skill in the art to implement the teaching of Johansen into Groen as to assure that the DCR would always be kept within its lock-in range in relation to an expected bit rate of the incoming data stream as taught by Johansen (see col.18, lines 1-15).

As per claim 7, Johansen teaches wherein the reference clock signal processing circuitry further comprises: a parts per million detector operative to output a signal

indicative of when a frequency difference between the reference clock signal and an output signal of the divider circuit is within a predetermined frequency setting (see col.17, lines 54-67).

It would have been obvious tone of ordinary skill in the art to implement the teaching of Johansen into Groen as to assure that the DCR would always be kept within its lock-in range in relation to an expected bit rate of the incoming data stream as taught by Johansen (see col.18, lines 1-15).

As per claim 8, Johansen teaches wherein the predetermined frequency setting is dynamically adjustable (see col.17, lines 54-67).

It would have been obvious tone of ordinary skill in the art to implement the teaching of Johansen into Groen as to assure that the DCR would always be kept within its lock-in range in relation to an expected bit rate of the incoming data stream as taught by Johansen (see col.18, lines 1-15).

As per claim 29, Groen et al teaches further comprising automatically switching from processing in reference clock mode to processing in data mode when the first signal is set to a first logic value, when the second signal is set to a second logic value, and when a frequency difference between the reference clock signal and the recovered clock signal is within a predetermined frequency setting.

30. The method of claim 29 wherein the predetermined frequency setting is dynamically adjustable.

31. The method of claim 28 further comprising automatically switching from processing in data mode to processing in reference clock mode when the first signal is set to a first

logic value, when the second signal is set to a second logic value, and when a problem is detected during the processing in data mode.

Allowable Subject Matter

5. Claims 20-25 are allowed over the prior art of record.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior arts of record fail to anticipate or render obvious the following recited features: **control circuitry that receives as input a first signal, a second signal, and the output signal of the PPM detector and is operative to control the reference clock signal processing circuitry and the data recovery circuitry** as recited in claim 20.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. ***

Laturell et al U.S. Pub No 2004/0096013 A1 teaches a clock and data recovery.

Black et al U.S. Pub No 2005/0058222 A1 teaches an analog front end.

Robinson et al U.S. Patent No 7,133,648 B1 teaches a bidirectional multi-gigabit transceiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Bayard
Primary Examiner
Art Unit 2611

11/8/06

EMMANUEL BAYARD
PRIMARY EXAMINER